What is claimed is:

1. A packet processing apparatus for converting packet data through a plurality of layers, comprising:

a packet memory for storing the entire packet; and

a shared memory for storing part of each packet of the packet data used in processes of a lower layer processing portion and a higher layer processing portion, the lower layer processing portion and the higher layer processing portion accessing the same memory space of said shared memory through physically different memory buses.

2. A packet processing apparatus for exchanging packet data through a plurality of layers, comprising:

a packet memory for storing the entire packet; and

a shared memory as a multi-port memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of said shared memory, wherein the layer 2 and 3 are recommended by Open System Interconnection reference model.

3. The packet processing apparatus as set forth in claim 2, further comprising:

a layer 2 reception processing portion for storing only a field necessary for layer 3 or a higher layer to said packet memory and said shared memory.

4. The packet processing apparatus as set forth in claim 1, further comprising:

a layer 2 transmission processing portion for combining data

stored in a plurality of packet memories and data stored in said shared memory and transmitting the resultant data as the packet, wherein the layer 2 is recommended by Open System Interconnection reference model.

5. A packet processing method for exchanging packet data through a plurality of layers, comprising the steps of:

storing the entire packet to a packet memory; and

storing part of each packet of the packet data used in processes of a lower layer processing portion and a higher layer processing portion of the plurality of layers to a multi-port shared memory, the lower layer processing portion and the higher layer processing portion accessing the same memory space of the multi-port shared memory.

6. A packet processing method for exchanging packet data through a plurality of layers by recommended Open System Interconnection reference model, comprising the steps of:

storing the entire packet to a packet memory; and

storing part of each packet of the packet data used in processes of a layer 2 processing portion and a layer 3 processing portion to a multi-port shared memory, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of the multi-port shared memory.

7. The packet processing method as set forth in claim 6, wherein a pipeline processing system is used so that the layer 2 processing portion and the layer 3 processing portion access the shared memory without an interference.

8. A packet exchange for exchanging packet data through a plurality of layers, comprising:

a packet memory for storing the entire packet; and

a multi-port shared memory for storing part of each packet of the packet data used in processes of a lower layer processing portion and a higher layer processing portion of the plurality of layers, the lower layer processing portion and the higher layer processing portion accessing the same memory space of said multi-port shared memory.

9. A packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model, comprising:

a packet memory for storing the entire packet; and

a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of said multi-port shared memory.

10. The packet exchange as set forth in claim 9, further comprising:

a processor, connected to said layer 2 processing portion and said layer 3 processing portion, for executing a process of a layer higher than layer 3.

11. A packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model, comprising:

a layer 2 reception processing portion for receiving a packet, storing the received packet to a packet memory, and storing a header portion of the received packet to a shared memory;

a layer 3 processing portion for receiving the header portion, executing a network process corresponding to the header portion, updating the header portion when necessary, and storing the updated header portion to the same address of said shared memory; and

a layer 2 transmission processing portion for combining the updated header portion received from said layer 3 processing portion and stored in said shared memory and packet information stored in said packet memory and transmitting the resultant data as a packet.

12. The packet exchange as set forth in ~~claim 11~~,

wherein said layer 2 transmission processing portion combines data updated by said layer 3 processing portion and stored in said shared memory and packet data stored in said packet memory, transmits the combined data, converts a packet format into a format of layer 1, and when layer 3 is an IP (Internet Protocol) layer, converts an IP V4 (Version 4) packet into an IP V 6 (Version 6) packet or vice versa.

13. The packet exchange as set forth in claim 11,

wherein said layer 2 transmission processing portion combines data updated by said layer 3 processing portion and stored in said shared memory and packet data stored in said packet memory by said layer 2 reception processing portion, and when layer 3 is an IP (Internet Protocol) layer, performs an IP V6 tunneling process for an IP V4 packet (namely, an IP V6 header is added to or deleted from an IP V4 packet), an IP V4 tuning process for an IP V6 packet (an IP V4 header is added to or deleted from an IP V6 packet), or an IP V4 tunneling process for an IP V4 packet (an IP V4 packet is added to or deleted from an IP V4 packet).